**Lesson Plan**

**Name of the Teacher**: Himani Vaidya  **Subject** : Computer organization and Architecture

**Semester: 4th** Semester Comp Engg **Session:**  Feb-July, 2023

**Month: February**

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| **Sr. No.** | **Week** | **Date** | **Name of the Chapter** | **Contents to be taught** | **Remark** |
|  | 3 | 14th,15th,16th  | Unit-1:Introduction | * Brief history of computers,
* Block Diagram of Digital Computers, Computer Organization,
 |  |
|  | 4 | 20th,21st,22nd,23rd  | Unit-1:Introduction | * Computer Design and Computer Architecture,
* Von Neumann Architecture.
 |  |
|  | 5 | 27th,28th  | Unit -2 : Computer Architecture | * Addition and Subtraction with Signed-Magnitude Data - Hardware Implementation and Algorithm.
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**Signature of Teacher**

**Himani Vaidya**

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**Semester: 4th** Semester Comp Engg **Session:**  Feb-July, 2023

**Month: March**

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| **Sr. No.** | **Week** | **Date** | **Name of the Chapter** | **Contents to be taught** | **Remark** |
|  | 1 |  1st,2nd  | Unit -2 : Computer Architecture | * Addition and Subtraction with 2's Complements Data - Hardware for 2's complement addition and subtraction.
 |  |
|  | 2 | 6th,9th  | Unit -2 : Computer Architecture | * Algorithm for adding and subtracting numbers in 2's complement representation.
 |  |
|  | 3 | 13th,14th, 15th, 16th  | Unit -2 : Computer Architecture | * Multiplication Algorithms - Hardware Implementation for Signed-Magnitude Data
* Booth Multiplication Algorithm.
 |  |
|  | 4 | 20th, 21st,22nd , 23rd  | Unit-3: Central Processing Unit | * Components of CPU,
* General Register Organization,
* Stack Organization - Register and Memory Stack,
 |  |
|  | 6 | 27th,28th, 29th  | Unit-3: Central Processing Unit | * Reverse Polish Notation and Evaluation of Arithmetic Expressions; Instruction formats Three Address Instructions, Two Address Instructions, One Address Instructions, Zero Address Instructions;
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**Semester: 4th** Semester Comp Engg **Session:**  Feb-July, 2023

**Month: April**

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| **Sr. No.** | **Week** | **Date** | **Name of the Chapter** | **Contents to be taught** | **Remark** |
|  | 1 | 3rd, 4th, 5th, 6th  | Unit-3: Central Processing Unit | * Brief Introduction to RISC and CISC;

Microprogrammed Vs Hardwired Control Units |  |
|  | 2 | 10th, ,11th,12th ,13th | Unit-4:Memory Organization | * Memory Devices Characteristics
* Memory Hierarchy,
* Main Memory (RAM & ROM),
 |  |
|  | 3 | 17th,18th,19th, 20st  | Unit-4:Memory Organization | * Introduction to Associative Memory,Cache Memory - Locality of Reference, Hit Ratio,
* Writing into Cache - Write Through, Write Back
 |  |
|  | 4 | 24th ,25th, 26th, 27th  | Unit-5: Input-Output Organization | * Peripheral Devices.
* Input-Output Interface
* I/O Versus Memory Bus
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**Semester: 4th** Semester Comp Engg **Session:**  Feb-July, 2023

**Month: May,June**

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| **Sr. No.** | **Week** | **Date** | **Name of the Chapter** | **Contents to be taught** | **Remark** |
|  | 1 | 1st,2nd, 3rd ,4th | Unit-5: Input-Output Organization | * Isolated versus Memory-Mapped I1O;

Modes of Transfer - Programmed I1O, Interrupt-Initiated I/O and DMA. |  |
|  |  | 8th, 9th ,10th,11th  |  | House test |  |
|  |  | ,15th 16th,17th, 18th | Unit-6:8085 Microprocessor | * Features, Block Diagram,
* Registers,
* Address Bus, Data Bus
 |  |
|  |  |  23rd, 24th, 25th  | Unit-6:8085 Microprocessor | * Interrupts,
* Addressing Modes
 |  |
|  |  | 29th, 30th, 31st | Unit-6:8085 Microprocessor | * Instruction Set (Introduction only),
* Memory and I1O Interfacing
 |  |
|  |  | 1st, 5th, 6th, 7th, 8th  | Unit-6: Overview of Advanced Microprocessor | * Parallel Processing,
* Pipelining, Vector Processing,
* Hyper Threading
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